# KERALA TECHNOLOGICAL UNIVERSITY

## Master of Technology

Curriculum, Syllabus and Course Plan

| | | |
|---|---|---|
| ***Cluster*** | **:** | *1* |
| ***Branch*** | **:** | *Electronics & Communication* |
| ***Stream*** | **:** | *VLSI & Embedded Systems* |
| ***Year*** | **:** | *2015* |
| ***No. of Credits*** | **:** | *67* |

## SEMESTER 1

| Examination Slot | Course Number | Name | L-T-P | Internal Marks | End Semester Examination | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | | Marks | Duration (hours) | |
| A | 01EC6601 | Digital System Design | 3-0-0 | 40 | 60 | 3 | 3 |
| B | 01EC6603 | VLSI Technology and Design | 3-1-0 | 40 | 60 | 3 | 4 |
| C | 01EC6605 | Designing with Microcontrollers | 3-1-0 | 40 | 60 | 3 | 4 |
| D | 01EC6607 | Embedded and Real Time Systems | 3-0-0 | 40 | 60 | 3 | 3 |
| E | | Elective I | 3-0-0 | 40 | 60 | 3 | 3 |
| S | 01EC6999 | Research Methodology | 0-2-0 | 100 | | | 2 |
| T | 01EC6691 | Seminar I | 0-0-2 | 100 | | | 2 |
| U | 01EC6693 | Reconfigurable Computing Lab | 0-0-2 | 100 | | | 1 |
| | | **TOTAL** | **15-4-4** | **500** | **300** | **-** | **22** |

**TOTAL CONTACT HOURS : 23**
**TOTAL CREDITS : 22**

### Elective I

01EC6311 Speech Signal Processing
01EC6613 Electronic Design Automation Tools
01EC6615 Electronic System Design

## SEMESTER 2

| Examination Slot | Course Number | Name | L-T-P | Internal Marks | End Semester Examination | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | | Marks | Duration (hours) | |
| A | 01EC6602 | Analog Integrated Circuit Design | 3-1-0 | 40 | 60 | 3 | 4 |
| B | 01EC6604 | Advanced VLSI DSP Architectures | 3-0-0 | 40 | 60 | 3 | 3 |
| C | 01EC6606 | Embedded System Design | 3-0-0 | 40 | 60 | 3 | 3 |
| D | | Elective II | 3-0-0 | 40 | 60 | 3 | 3 |
| E | | Elective III | 3-0-0 | 40 | 60 | 3 | 3 |
| V | 01EC6692 | Mini Project | 0-0-4 | 100 | | | 2 |
| U | 01EC6694 | Advanced Micro Controller Lab | 0-0-2 | 100 | | | 1 |
| | | **TOTAL** | **15-1-6** | **400** | **300** | **-** | **19** |

**TOTAL CONTACT HOURS : 22**
**TOTAL CREDITS : 19**

### Elective II

01EC6612 System on Chip Design
01EC6614 Fundamentals of Mechatronics
01EC6616 Embedded Linux Systems

### Elective III

01EC6618 Functional Verification with SystemVerilog
01EC6622 High Speed Digital Design
01EC6624 Nanoelectronics: Devices & Materials

## SEMESTER 3

| Examination Slot | Course Number | Name | L-T-P | Internal Marks | End Semester Examination | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | | Marks | Duration (hours) | |
| A | | Elective IV | 3-0-0 | 40 | 60 | 3 | 3 |
| B | | Elective V | 3-0-0 | 40 | 60 | 3 | 3 |
| T | 01EC7691 | Seminar II | 0-0-2 | 100 | | | 2 |
| W | 01EC7693 | Project (Phase 1) | 0-0-12 | 50 | | | 6 |
| | | **TOTAL** | **6-0-14** | **230** | **120** | **-** | **14** |

**TOTAL CONTACT HOURS : 20**
**TOTAL CREDITS : 14**

### Elective IV

01EC7611 Low Power Digital Design
01EC7613 VLSI Testing
01EC7615 Innovative DSP Concepts

### Elective V

01EC7617 Static Timing Analysis: Constraints & Analysis
01EC7619 Nanoscale Transistors
01EC7621 VLSI Design Automation

## SEMESTER 4

| Examination Slot | Course Number | Name | L-T-P | Internal Marks | End Semester Examination | | Credit |
|---|---|---|---|---|---|---|---|
| | | | | | Marks | Duration (hours) | |
| W | 01EC7694 | Project (Phase 2) | 0-0-23 | 70 | 30 | | 12 |
| | | **TOTAL** | **0-0-23** | **70** | **30** | **-** | **12** |

**TOTAL CONTACT HOURS : 23**
**TOTAL CREDITS : 12**

## TOTAL NUMBER OF CREDITS: 67

# SEMESTER - I

Syllabus and Course Plan

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6601 | Digital System Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. This course covers topics in the advanced design and analysis of digital circuits.
2. The primary goal is to provide an in depth understanding of digital logic and digital system design using hardware description languages.
3. The course enables students to apply their knowledge for the design of advanced digital hardware systems with corresponding EDA tools**.**

## Syllabus

Introduction to Digital Systems Design, Design of combinational and sequential circuits, Sequential Circuit Design, Asynchronous sequential circuits, FPGA architecture, Designing with SM charts, VHDLBasics and HDL based design flow.

## Expected Outcome

1. The student will get a strong understanding of advanced digital design including synchronous and asynchronous sequential circuits.
2. The students will get a basic knowledge of VHDL language and about the VLSI Design flow targeted towards FPGA

## References

1. Charles H Roth Jr , Digital Design using VHDL, Cenage Publishers ,India Edition,2006.
2. J. Bhasker; A VHDL Primer, Pearson Education, 2000.
3. N.N Biswas, Logic Design Theory, Prentice Hall of India, 1st Edn.
4. Charles H. Roth, Fundamentals of Logic Design, Thomson Publishers, 5th edition.
5. Milos D Ercegovac, Tomas Lang, Digital systems and hardware / firmware algorithm, John Wiley, 1985.
6. Digital Design Fundamentals", Kenneth J Breeding, Prentice Hall, Englewood Cliffs, New Jersey.
7. John F Wakerly, Digital Design Principles and Practice –4th Edition, Pearson education, 2006

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | **Introduction to Digital Systems Design**: Design of combinational and sequential circuits using ROMs, PALs and PLAs, Arithmetic PAL devices – Study based on PAL22V10 | 7 | 15 |
| **II** | **Sequential Circuit Design:**Clocked Synchronous State Machine Analysis, Mealy and Moore machines.<br>Finite State Machine design procedure – derive state diagrams and state tables, state reduction methods, and state assignments.<br>Design examples using the FSM approach –sequence detector, serial adders, multipliers | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Asynchronous sequential circuits:** Analysis, Derivation of excitation table, Flow table reduction, State assignment, Transition table, Design of asynchronous Sequential circuits, Race conditions and cycles, Static and dynamic hazards, Essential hazards, Methods for avoiding races and hazards. | 7 | 15 |
| **IV** | **FPGA architecture** – RAM based FPGAs - Antifuse FPGAs - Selecting FPGAs – CLBs, Input/output Blocks - Programmable Interconnect (study based on Xilinx FPGAs only). Dedicated Specialized Components of FPGAs, Applications of FPGAs. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Designing with SM charts**– State machine charts, Derivation of SM charts and Realization of SM charts. Implementation of Binary Multiplier, dice game controller. | 7 | 20 |
| **VI** | **VHDL Basics** - Introduction to HDL - Behavioral modeling - Data flow modeling- Structural modeling - Basic language elements, HDL based design flow. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6603 | VLSI Technology & Design | **3-1-0** | **4** | **2015** |

## Course Objectives

1. To study MOSFET and its characteristics, IC processing steps in detail.
2. To understand the concepts of CMOS invertors and its logic styles, memory design.
3. Enables the student to draw stick diagrams and make them familiar with Design rules and scaling methods.

## Syllabus

Review of Microelectronics and Introduction to MOS Technologies- MOS Transistor Theory, MOSFET Scaling and Small Geometry effects. IC Processing Steps- Crystal growth and wafer preparation, Epitaxy, Oxidation, Lithography, Etching techniques , Film deposition, Diffusion, Ion implantation, Metallization, VLSI Process Integration. Basics of Digital CMOS Design- The MOS Inverter- Power Consumption- Latch-up in CMOS circuits- Ratioed and Pass Transistor logic- Arithmetic circuits in CMOS VLSI. Sequential MOS Logic Design-Static and Dynamic FlipFlops and Latches, Memory Design, Domino and NORA logic. Circuit design Process: Circuit elements- Resistor , Capacitor, Stick diagrams, Design rules and layout, scaling of MOS circuits.

## Expected Outcome

1. The student will develop a strong understanding of the concepts of MOSFETS, CMOS Inverters, IC Processing Steps and various Logic Design Styles discussed.
2. The student will be able to design CMOS based circuits by drawing the stick diagram and applying various design rules & scaling methods discussed.

## References

1. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Pearson Education, Second Edition, 2003.
2. S.M.Sze,VLSI Technology, McGraw Hill Book Company, second Edition,2003.
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, Tata MGH, 3rd edition.2003.
4. Douglas A Pucknell& Kamran Eshragian , Basic VLSI Design, PHI, Third Edition.
5. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective," 2nd edition, Pearson Education (Asia) Pte. Ltd, 2000.

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | **Review of Microelectronics and Introduction to MOS Technologies:**Technology trends, VLSI Design Flow. MOS Transistor Theory: n MOS / p MOS transistor-Structure and operation, threshold voltage equation, body effect, MOSFET Current-Voltage Characteristics: Gradual Channel Approximation, Channel length modulation. MOS device design equation**,** MOSFET Scaling and Small Geometry effects. | **9** | 15 |
| **II** | **IC Processing Steps-Part I:**Crystal growth and wafer preparation-EGS, Czochralski Crystal Growing, Silicon Shaping, Processing considerations. Epitaxy-Types. Oxidation-Growth mechanism and kinetics, Thin Oxides, Oxidation Techniques & systems. Lithography-Types. Etching techniques-Types- Reactive Plasma Etching-Plasma Properties, Etching Techniques & Equipment | 9 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **IC Processing Steps-Part II:**Film deposition-Physical & Chemical Vapour Deposition methods & equipment, Dielectric &Polysilicon film deposition-Deposition Variables, Properties & methods. Diffusion-Diffusion models, Flick's 1D diffusion equations, Atomic Diffusion mechanisms, Measurement Techniques. Ion implantation-Method, Range theory, Equipment. Metallization-properties, Application, methods, patterning, VLSI Process Integration NMOS, CMOS, Bipolar and BICMOS. | 9 | 15 |
| **IV** | **Basics of Digital CMOS Design:**The MOS Inverter: principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. Latch-up in CMOS circuits. Ratioed logic, Pass Transistor logic, Arithmetic circuits in CMOS VLSI-Adders, multipliers, shifters. | 10 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Sequential MOS Logic Design:**Static latches; Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design, SRAM and DRAM, Domino and NORA logic. | 10 | 20 |

| | | | |
|---|---|---|---|
| **VI** | **Circuit design Process :**Circuit elements- resistor , capacitor, interconnects: sheet resistance , standard unit capacitance and unit delay concepts, inverter delays, driving capacitive loads, propagation delays; MOS layers, Stick diagrams; Design rules and layout- Lambda Based Design rules- micron based design rules; scaling of MOS circuits. | 9 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6605 | Designing with Microcontrollers | **3-1-0** | **4** | **2015** |

## Course Objectives

1. To understand the architectures of Intel 8051, PIC 16F87X microcontrollers, ARM processor.
2. To familiarize with the design and development process of embedded systems based on these microcontrollers

## Syllabus

Basic Intel 8051 and PIC 16F87X microcontroller's architecture- peripherals - programming in assembly level language; Basics of ARM Cortex M3 - exceptions, interrupts, NVIC, operation modes; The tool chain for developing a microcontroller based embedded system, the IDE environment, Applications of 8 bit microcontroller by interfacing it with real world devices.

## Expected Outcome

1. The student will get a strong understanding of general purpose microcontrollers.
2. Lead the student to the new overgrowing microprocessor architectural advancements through ARM and keep them familiarized with its new architectural advancements.
3. The student will become familiar about the use of microcontroller in solving real world issues.

## References

1. Ayala Kenneth J, 8051 microcontroller: Architecture, Programming and Application, 3rd edition
2. PIC 16F87X datasheet.
3. Joseph Yiu, The Definitive Guide to the ARM Cortex- M3,2nd edition , Newness.
4. Muhammad Ali Mazidi, R.D.Mckinlay, The 8051 Microcontroller and Embedded Systems using Assembly & C, 2nd Edition, Pearson Education
5. Muhammad Ali Mazidi, R.D.Mckinlay, PIC Microcontroller and Embedded Systems using Assembly & for PIC 18, sixth Edition, Pearson Education.
6. Cortex-M3 Technical Reference Manual, ARM Limited.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **8051 Microcontroller:**Architecture: CPU Block diagram, Memory organization, Program memory, Data memory, Interrupts.<br>Peripherals:- Timers, Serial port & I/O Port. Addressing Modes, Instruction Set, Assembly level Programming using 8051. | 9 | 15 |
| II | **PIC 16F 87X Microcontroller:**CPU Architecture - Block diagram, Memory organization, Program memory, Data memory, Interrupts, Addressing Modes, Instruction Set.<br>**Peripherals:-** Timers, Watch dog timer, ADC ,Synchronous Serial port, I/O Port, Power on Reset and Brown out reset, Programming using PIC 16F87X | 9 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **ARM Processor basics:**ARM Cortex-M3 Processor, Background of ARM and ARM Architecture, Instruction Set Development, The Thumb-2 Technology and Instruction Set Architecture.<br>**Overview and basics of the Cortex-M3 :**Registers , Special Registers , Operation Modes , Switching the operation modes ,The Built-In Nested Vectored Interrupt Controller ,The Memory Map ,The Bus Interface, The MPU ,The Instruction Set , Switching between ARM Code and Thumb Code in Traditional ARM Processors ( ARM7), Debugging Support. | 9 | 15 |
| IV | **ARM Cortex M3 Memory Systems:**Memory Maps, Bit-Band Operations, Unaligned Transfers, Exclusive Accesses, Endian Mode. Cortex-M3 Implementation Overview: The Pipeline, A Detailed Block Diagram. Bus Interfaces on the Cortex-M3, The External PPB, Reset Types and Reset Signals. **Exceptions :**Exceptions and Interrupts, Vector Tables ,Stack Memory Operations,Exception Types, Definitions of Priority, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call. | 10 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Microcontroller based System Development tools :** Tool chain for embedded system development , host and target machines, IDE, Cross assembler, Cross compiler, simulators , Debuggers, Emulators- ICE, JTAG &OnCE , Logic Analyzers , Oscilloscope | 9 | 15 |

| | | | |
|---|---|---|---|
| **VI** | **Microcontroller based System Design:**Case study with reference to a popular 8 bit microcontroller. A typical application design from requirement analysis through concept design, detailed hardware and software design using 8 bit microcontroller(s) to demonstrate the use of Interrupts and available peripherals, interfacing them with real world devices such as ADC, DAC, sensors etc. | 10 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6607 | Embedded and Real Time Systems | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the basic concepts of an embedded system , how it offers a real time response to a problem, what are the services offered by the operating system that helps them to meet the strict deadlines, how to meet the various constraints of an embedded software , from a programmer's perspective ,different stages of software development etc.

## Syllabus

Review of Embedded Systems, basic peripherals , Interrupts and its significance in real time processing, Pros and Cons of various software architectures , Introduction to RTOS, semaphores and shared data, other operating system services including mailboxes, pipes, message queues, interrupt routine in RTOS environment, developing embedded software and the various process involved, mostly used data structures within the embedded system software.

## Expected Outcome

1. This course provides the essential knowledge about an embedded system as well as the structure of a RTOS.
2. This enables the student to be familiar with the various aspects of efficient software coding, thus making them to think about meeting the several constraints of an embedded system design.
3. This course also provides some interesting and in-depth analysis of many real time embedded coding that may end up in failures without any certainty, and thus enables the students to expand their coding standards.

## References

1. Steve Heath, Embedded System Design, 2nd edition, Newnes.
2. David Simon Embedded Software Primer, Addison- Wesley, 1999.
3. Dr.K V K K Prasad, Embedded / Real time systems: Concepts, Design and Programming, Dream Tech press, New Delhi.
4. Frank Vahid,Tony D. Givargis, Embedded System Design- A Unified Hardware/ Software Introduction, John Wiley and Sons, Inc 2002.
5. D Jonathan W. Valvano,Embedded Microcomputer systems, Brooks / Cole, Thompson Learning. New Jersey.
6. Arnold S Burger, Embedded Systems Design - Introduction to Processes, Tools, Techniques", CMP books

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | **Introduction to Embedded Systems:**What it is ? Inside the embedded system? Categories of embedded systems, overview of embedded system architecture; specialties of embedded systems recent trends in embedded systems.**Memory Systems**- memory technology, RAM, EPROM and OTP, memory organization, error detecting and correcting memory, access times, packages, DRAM interfaces, DRAM refresh techniques, Cache coherency , Bus Snooping, MESI , MEI protocols, big and little Endian memory ,dual port and shared memory, memory overlays, shadowing. | 7 | 15 |
| **II** | **Basic Peripherals-** parallel port, timers/counters, real time clocks, serial ports, SPI , I2C, RS232, UART RS 422/RS485, USB, IEEE1394, Bluetooth, Zigbee, Wifi, CAN. **Real Time Operating Systems:-**what are Operating Systems, Operating System Internals, multitasking Operating Systems, Scheduler Algorithms, Commercial OS, Resource Protection, LINUX, Disk Partitioning. | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Interrupts** and its significance in real time processing- saving and restoring context, disabling interrupts, characteristics of shared data, atomic and critical sections interrupt latency.<br>**Survey of software Architectures:**Round Robin, Round Robin with interrupts, Function Queue scheduling Architecture, RTOS Architecture, Architecture selection, Introduction to RTOS,- Task and task states, Task and data, Semaphore and shared data. | 7 | 15 |
| **IV** | **More operating system services** - Message Queues, Mail boxes and pipes, Timer functions, events, Memory Management, Interrupt routine in an RTOS environment. **Basic Design using an RTOS:**Principle, Encapsulating Semaphores and Queues, Hard Real-Time scheduling considerations, saving memory space, saving power | 7 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Embedded Software Development Tools:-**Host and Target Machines, Linker/ Locator for Embedded Software , Getting Embedded Software into the target system, Debugging Techniques, Testing on your host machine, Instruction Set Simulators, The Assert Macro, Using | 7 | 15 |

| | | | |
|---|---|---|---|
| | Laboratory tools. | | |
| **VI** | **Writing Software for Embedded Systems:-**The compilation process, Native versus cross compilers, Run time libraries, Writing a library, Using alternative libraries, Using a standard library, Porting Kernels, C extensions for Embedded Systems<br>**Buffering and other data structures**-Linear buffer, Directional buffer, Double buffering, Buffer exchanging, Linked lists, FIFO, Circular buffers, Buffer under run and overrun, Allocating buffer memory, memory leakage.. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6311 | Speech Signal Processing | **3-0-0** | **3** | **2015** |

## Course Objectives

1. Familiarize the basic mechanism of speech production and get an overview of articulatory and acoustic Phonetics.
2. Learn the basic concepts of methods for speech analysis and parametric representation of speech.
3. Acquire knowledge about various methods used for speech coding.
4. Get an overall picture about various applications of speech processing.

## Syllabus

Speech production, Articulatory and Acoustic phonetics, Time domain analysis, Frequency domain analysis, Cepstral analysis, LPC analysis, GMM, HMM, Speech coding, Speech recognition, Speech enhancement, Text to speech

## Expected Outcome

1. Understand basic concepts of speech production, speech analysis, speech coding and parametric representation of speech and apply it in practical applications.
2. Ability to develop systems for various applications of speech processing.

## References

1. Douglas O'Shaughnessy, Speech Communications: Human & Machine, IEEE Press, Hardcover 2nd edition, 1999; ISBN: 0780334493.
2. Nelson Morgan and Ben Gold, Speech and Audio Signal Processing: Processing and Perception Speech and Music, July 1999, John Wiley & Sons, ISBN: 0471351547.
3. Rabiner and Schafer, Digital Processing of Speech Signals, Prentice Hall, 1978.
4. Rabiner and Juang, Fundamentals of Speech Recognition, Prentice Hall, 1994.
5. Thomas F. Quatieri, Discrete-Time Speech Signal Processing: Principles and Practice, Prentice Hall; ISBN: 013242942X; 1st edition.
6. Donald G. Childers, Speech Processing and Synthesis Toolboxes, John Wiley & Sons, September 1999; ISBN: 0471349593.

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | **Speech Production:** Acoustic theory of speech production (Excitation, Vocal tract model for speech analysis, Formant structure, Pitch). Articulatory Phonetics, and Acoustic Phonetics, Speech Analysis: Short-Time Speech Analysis, Time domain analysis (Short time energy, short time zero crossing Rate, ACF). | 7 | 14 |
| **II** | **Frequency domain analysis** (Filter Banks, STFT, Spectrogram, Formant Estimation & Analysis), CepstralAnalysis**,** MFCC | 8 | 16 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Parametric representation of speech:** AR Model, ARMA model. LPC Analysis (LPC model, Auto correlation method, Covariance method, Levinson-Durbin Algorithm, Lattice form). | 8 | 18 |
| **IV** | **Sinusoidal Model,** GMM, Hidden Markov Model | 5 | 12 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Speech coding:** Phase Vocoder, LPC, Sub-band coding, Adaptive Transform Coding, Harmonic Coding, Vector Quantization based Coders, CELP. | 7 | 20 |
| **VI** | **Speech processing:** Fundamentals of Speech recognition, Speech segmentation. Text-to-speech conversion, speech enhancement, Speaker Verification, Language Identification, Issues of Voice transmission over Internet. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6613 | Electronic Design Automation Tools | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the basic methodology of Digital and Analog system design.
2. To know the EDA tool concepts used for electronic system design for IC and PCB.
3. To understand the different assembly and packaging techniques for ICs.

## Syllabus

Concept of EDA - Digital Simulation – Synthesis - Formal Verification - Design for Testability - Library Design - ASICs - Geometric layout (digital) - Geometric Verification - Analog Simulation - Mixed Signal Simulation - Geometric layout (CMOS) - Assembly & packaging Methods - PCB Design.

## Expected Outcome

1. The student will develop a strong understanding of the digital, analog and mixed signal IC design methodologies.
2. The student will be familiarized with the fundamental concepts of the tools required in the IC / electronic system design flow.

## References

1. Jansen, Dirk,"The Electronic Design Automation Handbook", 2003.
2. MironAbramovici, Melvin A.Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.
3. ORCAD: Technical Reference Manual, Orcad, and USA.
4. M.J.S.Smith.,"Application-Specific Integrated Circuits", Addison Wesley.
5. Jan M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits- a Design perspective", Pearson education/ Prentice-Hall India Ltd, 2nd edition.
6. M.H.Rashid,"SPICE FOR Circuits And Electronics Using PSPICE", Prentice Hall, 2nd edition.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Concept of EDA:** Design Methodology, Development steps, Implementation and Verification, Top Down or Bottom Up,Short history of EDA.<br>**Digital Simulation :**Why?, Simulation Model, SDF, Structure of a Digital Simulator, Fault simulation, Performance & Use of logic simulation, Verification of Testability with Simulation, Limits of Digital Simulation. | 7 | 15 |
| II | **Synthesis:** Introduction, Examples, Partitioning, Modification of Hierarchy, Optimization, Retiming, Technology mapping. Formal Verification: Model checking, Equivalence checking, Fundamental techniques, Sequential circuits, Correctness of Synthesis steps, Design verification. | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Design for Testability Fundamentals:**Faults in Digital circuits and their modeling, Fault simulation and fault collapsing, Digital test pattern generation–ATPG, ATPG algorithms, ATPG- Vector Formats and Compaction and Compression. Scan Architectures- Testability, Scan Registers, Generic scan based designs, Boundary Scan-JTAG. Built in Self Test (BIST) - BIST concepts and test pattern generation | 7 | 15 |
| IV | **Library Design:** Digital libraries, Pad cell Libraries, Analogue libraries, Macro Libraries.**ASICs:**Design goals for ASICs, Design Styles.<br>**Geometric layout::** Standard cell Layouts, LEF data format, GDSII format.<br>**Geometric Verification:**Introduction, Layer preprocessing, Design Rule check, Extract, Extraction of parasitic capacitors and resistors, ERC, LVS. | 7 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Analog Simulation:**Spice concept, Spice transistor models, Models of Operational Amplifiers, Analysis of Loop gain as Stability Criterion of Analog Circuits. **Mixed Signal Simulation:** Overview, Simulation on different levels of abstraction, Concept of Mixed signal simulators<br>**Geometric layout:**Layout of CMOS circuits | 7 | 20 |

| | | | |
|---|---|---|---|
| **VI** | **Assembly & packaging Methods:**Die Assembly, Electrical connections, Packaging Methods. **PCB Design:**PCB design flow, Schematic entry for PCB design, PCB layout | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6615 | Electronic System Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the factors influencing the Electronic System Design & Electromagnetic Compatibility issues in detail.
2. Enable the student to familiarize with different protection techniques developed to overcome the effect of noise & EMI.

## Syllabus

Introduction to Electronic System Design: Packaging & Enclosures of Electronic System, Effect of environmental factors on electronic system, Cooling in of Electronic System. Electromagnetic Compatibility: Designing for EMC, EMC regulations; Intrinsic Noise Sources-Measuring Random noise, Active Device Noise- Noise Factor & S/N Ratio, Bipolar transistor noise, JFET noise, Noise in IC operational Amplifiers; Cabling of Electronic Systems; Grounding; Balancing & Filtering; Shielding of Electronic Systems ; Protection against Electrostatic Discharges; Digital Circuit Noise & Layout; Digital Circuit Radiation: Differential-mode & Common mode Radiation & Controlling; PCB Design-Layout, General Rules & Parameters-Design Rules for Digital & Analog circuit PCBs.

## Expected Outcome

1. The student will be able to develop a strong understanding of the concepts of the noise sources which affects the system design & the methods adapted to overcome it.
2. The student gets familiarized with the PCB Design layout rules which have to be followed for designing Analog & Digital circuits.

## References

1. Kim R. Fowler; "Electronic Instrument Design", 1st edition; Oxford University Press.
2. Henry W. Ott, "Noise Reduction Techniques in Electronic Systems", 2nd edition; John Wiley & Sons.
3. Printed Circuit Boards-Design & Technology; by: W. Bosshart; Tata McGraw Hill.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Introduction to Electronic System Design:**Packaging & Enclosures of Electronic System, Effect of environmental factors on electronic system, Cooling in of Electronic System. **Electromagnetic Compatibility (EMC):** Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods for reducing interference in electronic systems. | 6 | 15 |
| II | **Intrinsic Noise Sources:** Thermal Noise, Short noise, Contact noise, popcorn noise, Addition of noise voltages, Measuring Random noise. **Active Device Noise:** Noise Factor & S/N Ratio, Optimum Source Resistance, Noise Temperature, Bipolar transistor noise, JFET noise, Noise in IC operational Amplifiers. | 6 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Cabling of Electronic Systems:** Capacitive & inductive coupling, effect of shield on capacitive, inductive and magnetic coupling, coaxial cable versus shielded twisted pair. Grounding; Balancing & Filtering. | 8 | 20 |
| IV | **Shielding of Electronic Systems; Protection against Electrostatic Discharges (ESD):** Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC. | 8 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Digital Circuit Noise & Layout::** Digital logic noise, Internal noise sources, Digital circuit ground noise, power distribution, Noise voltage objectives, Measuring noise voltages, Unused Inputs.**Digital Circuit Radiation:** Differential-mode Radiation & Controlling, Common mode Radiation & controlling. | 7 | 15 |
| VI | **PCB Design-Layout, General Rules & Parameters:** Resistance, capacitance & Inductance of PCB Conductors, conductor spacing, Realizing supply & ground conductors, cooling requirements & package density, Layout check.Design Rules for Digital circuit PCBs; Design Rules for Analog circuit PCBs. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6999 | Research Methodology | **0-2-0** | **2** | **2015** |

## Course Objectives

1. To prepare the student to do the M. Tech project work with a research bias.
2. To formulate a viable research question.
3. To develop skill in the critical analysis of research articles and reports.
4. To analyze the benefits and drawbacks of different methodologies.
5. To understand how to write a technical paper based on research findings.

## Syllabus

Introduction to Research Methodology-Types of research- Ethical issues- Copy right-royalty-Intellectual property rights and patent law-Copyleft- Openacess-
Analysis of sample research papers to understand various aspects of research methodology:
Defining and formulating the research problem-Literature review-Development of working hypothesis-Research design and methods- Data Collection and analysis- Technical writing- Project work on a simple research problem

## Approach

Course focuses on students' application of the course content to their unique research interests. The various topics will be addressed through hands on sessions.

## Expected Outcome

Upon successful completion of this course, students will be able to
1. Understand research concepts in terms of identifying the research problem
2. Propose possible solutions based on research
3. Write a technical paper based on the findings.
4. Get a good exposure to a domain of interest.
5. Get a good domain and experience to pursue future research activities.

## References

1. C. R. Kothari, Research Methodology, New Age International, 2004
2. Panneerselvam, Research Methodology, Prentice Hall of India, New Delhi, 2012.
3. J. W. Bames, Statistical Analysis for Engineers and Scientists, Tata McGraw-Hill, New York.
4. Donald Cooper, Business Research Methods, Tata McGraw-Hill, New Delhi.
5. Leedy P. D., Practical Research: Planning and Design, McMillan Publishing Co.
6. Day R. A., How to Write and Publish a Scientific Paper, Cambridge University Press, 1989.
7. Manna, Chakraborti, Values and Ethics in Business Profession, Prentice Hall of India, New Delhi, 2012.
8. Sople, Managing Intellectual Property: The Strategic Imperative, Prentice Hall ofIndia, New Delhi, 2012.

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | Introduction to Research Methodology: Motivation towards research - Types of research: Find examples from literature.<br><br>Professional ethics in research - Ethical issues-ethical committees. Copy right - royalty - Intellectual property rights and patent law - Copyleft-Openacess-Reproduction of published material - Plagiarism - Citation and acknowledgement.<br><br>Impact factor. Identifying major conferences and important journals in the concerned area. Collection of at least 4 papers in the area. | 5 | |
| **II** | Defining and formulating the research problem -Literature Survey-Analyze the chosen papers and understand how the authors have undertaken literature review, identified the research gaps, arrived at their objectives, formulated their problem and developed a hypothesis. | 4 | |
| **FIRST INTERNAL EXAM** | | | |
| **III** | Research design and methods: Analyze the chosen papers to understand formulation of research methods and analytical and experimental methods used. Study of how different it is from previous works. | 4 | No end semester written examination |
| **IV** | Data Collection and analysis.Analyze the chosen papers and study the methods of data collection used. - Data Processing and Analysis strategies used– Study the tools used for analyzing the data. | 5 | |
| **SECOND INTERNAL EXAM** | | | |
| **V** | Technical writing - Structure and components, contents of a typical technical paper, difference between abstract and conclusion,layout, illustrations and tables, bibliography, referencing and footnotes-use of tools like Latex. | 5 | |
| **VI** | Identification of a simple research problem – Literature survey-Research design- Methodology –paper writing based on a hypothetical result. | 5 | |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6691 | Seminar I | **0-0-2** | **2** | **2015** |

## Course Objectives

To make students

1. Identify the current topics in the specific stream.
2. Collect the recent publications related to the identified topics.
3. Do a detailed study of a selected topic based on current journals, published papers and books.
4. Present a seminar on the selected topic on which a detailed study has been done.
5. Improve the writing and presentation skills.

## Approach

Students shall make a presentation for 20-25 minutes based on the detailed study of the topic and submit a report based on the study.

## Expected Outcome

Upon successful completion of the seminar, the student should be able to

1. Get good exposure in the current topics in the specific stream.
2. Improve the writing and presentation skills.
3. Explore domains of interest so as to pursue the course project.

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6693 | Reconfigurable Computing Lab | **0-0-2** | **1** | **2015** |

## Course Objectives

1. To familiarize the FPGA design flow.

## Syllabus

HDL Programming using VHDL – Combinational and Sequential circuit design, use of state machines, Functional simulation, FPGA implementation Flow, Constraints, FPGA programming, Static Timing Analysis, Post-route Simulation, Design Debugging.

## List of Experiments

1. VHDL coding and functional simulation of a BCD counter.
2. Design, coding, functional simulation and synthesis of a FIFO
3. Design, coding, functional simulation and synthesis of a priority encoder that returns the codes of the highest and second-highest priority requests.
4. Realization of the following in the FPGA development board
5. 4-bit adder/subtractor in which inputs are given through 8 On/Off switches. The hexadecimal equivalent of these inputs along with the result should be displayed with the help of available LED displays. The addition/subtraction should be selectable with a push button switch.
6. FPGA implementation of a BCD counter with start and stop.
7. FPGA implementation of a pre-loadable gray counter.
8. Realization of a Real Time Clock in the FPGA development board.
9. Design, VHDL coding and implementation of a running display controller.
10. Design, VHDL coding and implementation of a voting machine.
11. Realization of a traffic light controller in the FPGA development board.

**Design of digital combinational and sequential circuits using VHDL and implementation on FPGA**

1. Familiarization of EDA Tools and FPGA Implementation
2. Combinational Circuit design, simulation, synthesis and implementation
3. Sequential Circuit design, simulation, synthesis and implementation
4. Mini Project on Digital System Design using VHDL

## Expected Outcome

1. Students will get familiarized with VHDL coding, FPGA implementation flow, Design Constraints and STA.

## References

1. J. Bhasker;"A VHDL Primer", Pearson Education, 2000.
2. J. Bhasker; "A VHDL Synthesis Primer", Second Edition.
3. http://www.xilinx.com/training/free-video-courses.htm.

# SEMESTER – II

Syllabus and Course Plan

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6602 | Analog Integrated Circuit Design | **3-1-0** | **4** | **2015** |

## Course Objectives

1. To gain an in depth knowledge of MOS transistors operations, characteristics and circuit design.
2. To familiarize and comprehend the design concepts and methodologies in analog CMOS circuit design.
3. Analysis and design of analog CMOS circuits starting from fundamental circuits and progressing to complex circuits including high gain amplifiers, switched capacitor circuits, clock generators etc.
4. To understand the concept and methodologies involved in the layout of analog circuits.

## Syllabus

MOS Device Basics and Operation, Basic MOS circuits, Frequency response and Noise, Operational Amplifiers, Advanced CMOS circuits, CMOS layout design

## Expected Outcome

1. The student will gain an in depth knowledge in the operation of MOS transistors.
2. The students will acquire the knowledge of the analysis and design of CMOS circuit.
3. The student will gain a glance in to the operation and design of advanced circuits.
4. The students will obtain knowledge into the concepts and methodologies of analog CMOS layout.

## References

1. BehzadRazavi, "Design of Analog CMOS Integrated Circuit", Tata McGraw HILL, 2002.
2. David. A. Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
3. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.
4. R. Jacob Baker, CMOS circuit Design Layout and Simulation, 3rd Edition.
5. Paul B Gray and Robert G Meyer, Analysis and Design of Analog Integrated Circuits 4th Edition.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **MOS Device Basics and Operation:** MOS I/V Characteristics - Threshold voltage, derivation of I/V characteristics, regions of operation; Second order effects; MOS Device Models - MOS device capacitances, large signal model, small signal model | 8 | 15 |
| II | **Basic MOS circuits:** Diode connected MOS - small signal equivalent, impedance; Common source amplifier -with resistive load, diode connected load, current source load, triode load, source degeneration; Source follower; Common gate stage; Cascode Stage; Current mirrors - basic passive current mirror, passive cascode current mirror; Differential amplifier- basic differential pair, analysis, common mode response. | 10 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Frequency response and Noise:** Frequency Response- bode plot, poles and zeroes, gain and phase margins, Miller effect, association of poles with nodes, analysis of common source amplifier frequency response; Noise- statistical characteristics of noise(noise spectrum, amplitude distribution, correlated and uncorrelated sources), types (thermal & flicker), noise bandwidth | 10 | 15 |
| IV | **Operational Amplifiers:** Performance parameters; One stage opamp- simple opamp, casocdeopamp, folded cascodeopamp; Two stage opamp - simple two stage opamp implementation, gain calculation; Common mode feedback- output common mode sensing (resistive feedback, source follower), common mode control in a folded cascode amplifier through simple amplifier; Frequency compensation- need for compensation, basic principle of compensation, miller compensation in two stage amplifier | 10 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Advanced CMOS circuits:** Temperature independent references- Negative-TC voltage, Positive TC voltage, Bandgap reference concepts; Phase Locked Loops-Simple PLL(topology and dynamics), Charge pump PLL(topology and dynamics), Non ideal effects in PLL, Delay | 9 | 20 |

| | | | |
|---|---|---|---|
| | Locked Loops, Applications of PLL; Switched capacitor circuits- Sampling switches, Unity gain buffer, non-inverting amplifier, switched capacitor integrator. | | |
| **VI** | **CMOS layout design:** General layout considerations -DRC, antenna effect; Analog Layout Techniques- Multifinger transistors, symmetry, reference distribution, passive devices, interconnects; Substrate coupling.. | 9 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6604 | Advanced VLSI DSP Architectures | **3-0-0** | **3** | **2015** |

## Course Objectives

Exposes the students to some of the advanced application domains of DSP including:

1. Sampling in the digital domain.
2. Adaptive systems and the several algorithms for adaptation..
3. Different transformation techniques that helps to meet the several constraints (area/speed/ power) of a digital system.
4. Algorithms for area efficient implementation of arithmetic structures.
5. Alternatives to synchronous design methodology aiming at improved throughput.

## Syllabus

Multirate system fundamentals, Applications of multirate signal processing, Adaptive Signal processing, Pipe lining and parallel processing, Transformations techniques-retiming, unfolding, folding, register minimization, Systolic Arrays, Fast convolution, Synchronous, wave and asynchronous pipelines.

## Expected Outcome

1. Develops a strong understanding of some of the advanced digital signal processing applications and how the Electronic Design Automation tools make use of the DSP techniques to meet the constraints of an efficient digital system.
2. Become familiar with other alternatives of synchronous design styles.

## References

1. Keshab K Parhi, VLSI DSP Systems- Design and Implementation – John Wiley, 2004..
2. LjiljanaMilić , Multirate Filtering for Digital Signal Processing - MATLAB applications, Information Science Reference,2009.
3. Bernard Widrow& Samuel D. Streams, Adaptive Signal Processing, Prentice Hall.
4. N J Fliege, Multirate Digital Signal Processing, John Wiley 1994.
5. P PVaidyanathan ,Multirate Systems And Filter banks,, Prentice Hall, PTR.
6. Emmanuel C Ifeachor, Barrie W. Jervis, Digital Signal Processing- A Practical Approach, Addison Wesley, 1993

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Multirate system fundamentals**: Basic Multirate operation – up sampling and down sampling, Time domain and frequency domain analysis, identities for multirate operations, Interpolator and decimator design, Rate conversion by non integer factor, polyphase structures, applications of multirate signal processing. | 7 | 15 |
| II | **Adaptive Signal processing:**Adaptive systems, Open and Closed Loop Adaptation, Adaptive Linear Combiner, Adaptive Algorithms and structures – LMS algorithm, Ideal LMS, Newton Algorithm and its properties, Advantages and disadvantages of adaptive recursive filters – LMS algorithm for recursive filters, Random search algorithms, Applications response. | 8 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Systolic Arrays-** Systolic array design methodology, FIR Systolic arrays, selection of scheduling vector, Matrix Matrix multiplications, 2 D systolic array design, Systolic design for space representations containing delays. | 7 | 15 |
| IV | **Synchronous, wave and asynchronous pipelines-**Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs, Wave pipelining, asynchronous pipelining. | 6 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Pipe lining and parallel processing-** pipe lining of FIR filters, Parallel processing, pipe lining and parallel processing for low power.**Fast convolution –** Cook Toom Algorithm, Modified Cook Toom Algorithm, WinogradAlgorithm, Iterated Convolution, Cyclic convolution. | 7 | 20 |
| VI | **Transformations techniques**- retiming- definitions and properties, retiming techniques, unfolding- algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, applications of unfolding, folding- folding transformation, register minimization techniques, register minimization in folded architectures. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6606 | Embedded System Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. This course gives knowledgeabout how to build an embedded system which meets requirements, while minimizing costs.
2. The course focuses on the design aspects of general purpose, single purpose and custom single purpose processors for an embedded system.
3. Also deals with advanced communication principles.
4. Also discuss about control systems and their computation models.
5. Illustrates the balance between hardware and software, with a suitable example.

## Syllabus

Embedded system overview, Design challenge, Design Technology, Memories, General-purpose Processors, Application, Selecting a Microprocessor/ General purpose Processor Design, Standard single-purpose processors, RT- level Custom Single purpose Processor Design, Advanced Communication Principles, Design and development of Digital Camera Example, Control Systems, Benefits of Computer Based Control Implementations.

## Expected Outcome

1. The student will understand the contemporary approach to embedded systems, as well as the integration concepts of software and hardware design.

## References

1. Frank Vahid and Tony Givargis, Embedded System Design-A Unified Hardware/Software Introduction", John Wiley & Sons, 2002.
2. Steve Heath, Butterworth Heinemann, "Embedded System Design."
3. Gajski and Vahid, "Specification and Design of Embedded systems", Prentice Hall.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| **I** | **Introduction:**Embedded system overview, Design challenge: Optimizing design metrics, IC Technology: Full- custom/VLSI, Semi-custom ASIC and PLD, Design Technology: Compilation/ Synthesis, Libraries/IP, Test/verification, Memories: ROM, RAM,Memory | 8 | 20 |

| | | | |
|---|---|---|---|
| | hierarchy and cache. | | |
| **II** | **General-purpose Processors:**Basic architecture, Datapath, Control unit, Memory, Pipelining, Superscalar and VLIW architectures. Application-Specific instruction-set Processors(ASIP's), Micro-controllers, DSP, Less-General ASIP environments, Selecting a Microprocessor/ General purpose Processor Design. | 8 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Single purpose Processor:**Standard single-purpose processors: Timers, counters, watchdog timers, UART, Pulse width Modulator, LCD controller, Keypad controller, Real time Clocks.RT- level Custom Single purpose Processor Design, Optimizing Custom Single- purpose Processors: Optimizing the original program, Optimizing the FSMD, Optimizing the datapath, optimizing the FSM. | 7 | 15 |
| **IV** | **Advanced Communication Principles:**Parallel, serial and wireless Communications, Serial protocols: The I2C Bus, The CAN bus, Fire wire bus, USB. Parallel protocols: PCI bus, AMBA bus, wireless protocols: IrDA , Bluetooth, IEEE 802.11 | 6 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Digital Camera Example:** User's perspective, Designer's perspective, Specification, Informal Functional specification, Non-functional specification. Executable specification. Design, Implementation: 8051-based design, Implementation, Fixed point FDCT, Implementation, Hardware FDCT. | 6 | 20 |
| **VI** | **Control Systems:**Open-loop and closed loop control systems, an open-looped automobile cruise controller, a closed-loop automobile cruise-controller, General control systems and PID controllers, Control objectives, Modeling real physical systems, Controller design, Fuzzy control. Practical Issues Related to Computer based Control, Benefits of Computer Based Control Implementations. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6612 | System on Chip Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand basics of System on Chip designs.
2. To understand the basic concepts of interconnections between processors and other components in a system environment.
3. To study the concepts of IP design and verification**.**
4. To understand fundamental concepts of Hardware/Software co-design.
5. To get a general idea about Multi processor SoCs.

## Syllabus

Introduction to System on Chips – major components, communication between components, standard protocols. The basic design concepts of a SoC, Different design approaches, System level design issues. Introduction to macro design process,Ttypes of macros, Design issues related to macros, Using reusable macros in a design. Hardware/Software Co-Design, SoC Verification, General approaches and concepts, Languages and methodologies. Basics of MPSoCs, Techniques for designing MPSoCs, MPSoC performance modeling and analysis. System-In-Package (SIP) design.

## Expected Outcome

1. The student will develop a strong understanding of SoCs, their design and verification.

## References

1. RochitRajsuman, "System-on-a-chip: Design and Test ", Artech House, 2000 ISBN..
2. Dirk Jansen,The EDA HandBook, Kluwer Academic Publishers.
3. MironAbramovici, Melvin A. Breur, Arthur D Friedman, Digital systems Testing and testable design, ISBN-13: 978-8172248918, Jaico Publishing House, 2001.
4. William K.Lam, Design Verification: Simulation and Formal Method based Approaches,Prentice Hall.
5. Stanley L. Hurst, VLSI Testing: digital and mixed analogue digital Techniques, Pub: Inspec /IEE, 1999.
6. A.A.Jerraya, W.Wolf, Multiprocessor Systems-on-chips, M K Publishers.
7. Reuse Methodology Manual for System-On-A-Chip Designs, Springer, 32nd Edition, 2007.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **System On Chip Introduction**:- Introduction to the concept of a SOC, SOC Architecture, SOC components, Hardware & Software, System level interconnection, System buses: Introduction to busses used in SOCs. Introduction to AMBA bus, Processors used in SOCs: Introduction to CISC, RISC, Von Neumann and Harward Architecture. Introduction to tools used for SOC design, Xilinx embedded design flow. | 6 | 15 |
| II | **System On Chip Design Process:-** A canonical SoC Design, SoC Design flow - waterfall vs. spiral, Top-down vs. Bottom up, Specification requirement, Types of Specification, System Design process, System level design issues- Soft IP vs. Hard IP, Design for timing closure, Logic design issues- Verification strategy. | 8 | 20 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Macro Design Process:-** Top level Macro Design, Macro Integration, Soft Macro productization, Developing hard macros, Design issues for hard macros, Design process, System Integration with reusable macros. | 7 | 15 |
| IV | **SoC Verification: -** Verification technology options, Verification methodology, Verification languages and methodologies, Verification approaches,Verification plans. System level verification, Block level verification, Hardware/software co-verification and Static net list verification. | 8 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Hardware/Software co-Design:** Concept of Design Reuse, Design with virtual components and processor cores, EDA systems for hardware/software co-designs, System on Chip Designs (SoC). | 6 | 15 |
| VI | **MPSoCs:** What, Why, How MPSoCs. Techniques for designing MPSoCs, MPSoC performance modeling and analysis. System-In-Package (SIP) design. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6614 | Fundamentals of Mechatronics | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To provide in-depth knowledge in the fundamentals, design, analysis and operation of mechatronic systems.

## Syllabus

Introduction to Mechatronics, fundamentals of electronics- Data conversion devices, sensors, microsensors, transducers, signal processing devices, relays, contactors and timers Drives, Hydraulic systems , design of Hydraulic systems,Physical Modelling , Simulation Techniques, modelling and simulation techniques for real world applications.

## Expected Outcome

1. The student will get familiarized to a multi-disciplinary area dealing with the integration of mechanical devices, actuators, sensors, electronics, intelligent controllers and computers.

## References

1. Dr. K. P. Ramachandran, Mechatronics: Integrated Mechanical Electronic Systems , Wiley India Pvt Ltd, 2008.
2. N.P MAHALIK , Mechatronics Prinicples Concepts & Applications, McGraw Hill Education (India) Private Limited, 1st Edition.
3. HMT ltd. Mechatronics, Tata Mcgraw-Hill, New Delhi, 1988.
4. G.W. Kurtz, J.K. Schueller, P.W. Claar. II, Machine design for mobile and industrial applications, SAE, 1994.
5. T.O. Boucher, Computer automation in manufacturing - an Introduction, Chappman and Hall, 1996.
6. R. Iserman, Mechatronic Systems: Fundamentals, Springer, 1st Edition, 2005.
7. Musa Jouaneh, Fundamentals of Mechatronics, 1st Edition, Cengage Learning, 2012.
8. L. Ljung, T. Glad, “Modeling of Dynamical Systems”, Prentice Hall Inc. (1994).
9. D.C. Karnopp, D.L. Margolis and R.C. Rosenberg, “System Dynamics: A Unified Approach”, 2nd Edition, Wiley-Interscience (1990).
10. G. Gordon, “System Simulation”, 2nd Edition, PHI Learning (2009).
11. V. Giurgiutiu and S. E. Lyshevski, “Micromechatronics, Modeling, Analysis, and Design with MATLAB”, 2nd Edition, CRC Press (2009).

| COURSE PLAN | | | |
|---|---|---|---|
| **Module** | **Contents** | **Hours Allotted** | **% of Marks in End-Semester Examination** |
| **I** | **Introduction:** Definition of Mechatronics, Mechatronics in manufacturing, Products, and design. Comparison between Traditional and Mechatronics approach. | 6 | 15 |
| **II** | **Review of fundamentals of electronics:** Data conversion devices, sensors, microsensors, transducers, signal processing devices, relays, contactors and timers. Microprocessors controllers & PLCs. | 6 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Drives:** stepper motors, servo drives. Ball screws, linear motion bearings, cams, systems controlled by camshafts, electronic cams, indexing mechanisms, tool magazines, transfer systems | 7 | 15 |
| **IV** | **Hydraulic systems:** flow, pressure and direction control valves, actuators, and supporting elements, hydraulic power packs, pumps. Design of hydraulic circuits. Pneumatics: production, distribution and conditioning of compressed air, system components and graphic representations, design of systems. Description. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Physical Modelling:** Mechanical and electrical systems, physical laws, continuity equations, compatibility equations, system engineering concept, system modelling with structured analysis, modelling paradigms for mechatronic system, block diagrams, mathematical models, systems of differential-algebraic equations, response analysis of electrical systems, thermal systems, fluid systems, mechanical rotational system, electrical-mechanical coupling. | 8 | 20 |
| **VI** | **Simulation Techniques:** Solution of model equations and their interpretation, zeroth, first and second order system, solution of 2nd order electro-mechanical equation by finite element method, transfer function and frequency response, non-parametric methods, transient, correlation, frequency, Fourier and spectra analysis.. | 8 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6616 | Embedded Linux Systems | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To familiarize the students with Linux System in Embedded world and to provide a deep knowledge about the Development systems and files systems.
2. Enable the student to understand the concepts of using memory of the systems and Drivers used for Embedded Linux.

## Syllabus

Introduction: Types of Embedded Linux systems, Examples of Embedded Linux systems- Processor architectures supported by Linux; Cross platform Development tool chain: GNU tool chain basics, Bootstrap Compiler Setup, Using the tool chain, C library alternatives, Terminal Emulators; Kernel and Root File System: Kernel Considerations, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, System Initialization; Storage Device Manipulation; Root File system Setup; Setting Up the Boot loader; Device Drivers- Introduction, Building and running modules, Char Drivers, Allocating memory, USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers.

## Expected Outcome

1. The student will develop a strong understanding of using the tool chain, concepts of file systems and device drivers discussed.

## References

1. KarimYaghmour, JonJasonBrittain and Ian F. Darwin Masters, Gilad Ben-Yossef, and Philippe Gerum**,** O'Reilly, Building Embedded Linux Systems 2nd Edition, 2008.
2. Alessandro Rubini, Jonathan Corbet, O'Reilly, Linux Device Drivers , 3rd Edition, 2005.
3. Christopher Hallinan, Embedded Linux Primer A Prctical Real – World Approch, Prentice Hall.
4. P Raghavan, Amol Lad, SriramNeelakandan, Embedded Linux System Design and Development, Auerbach Publications.
5. Alan Cox, Sreekrishnan , Venkateswaran, Essential Linux Device Drivers , Pretice Hall.
6. Craig Hollabaugh, Embedded Linux Hardware, Software and Interfacing, Pearson Education.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Introduction:** Embedded Linux, Real Time Linux, Types of Embedded Linux systems, Advantages of Linux OS, Using distributions, Examples of Embedded Linux systems- system architecture, Types of host/target architectures for the development of Embedded Linux Systems, Debug setups, Boot Configurations, Processor architectures supported by Linux. | 7 | 15 |
| II | **Cross platform Development Tool chain:**GNU tool chain basics, Kernel Headers Setup, Binutils setup, Bootstrap Compiler Setup, Library Setup, Full Compiler Setup, Using the tool chain, C library alternatives, JAVA, Perl, Python, Ada, IDEs , Terminal Emulators. | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Kernel and Root File System:**Kernel Considerations- selection, configuration , Compiling and Installing the kernel Root File System Structure, Libraries, Kernel Modules, Kernel Images, Device Files, Main System Applications, Custom Applications, System Initialization. | 6 | 15 |
| IV | **Storage Device Manipulation:**MTD-Supported Devices ,Disk Devices, Swapping.<br>**Root Filesystem Setup :**Filesystem Types for Embedded Devices, Writing a Filesystem Image to Flash using an NFS-Mounted Root Filesystem, Placing a Disk Filesystem on a RAM Disk , Rootfs and Initramfs, Choosing a Filesystem's Type and Layout, Handling Software Upgrades.<br>**Setting Up the Bootloader:**Embedded Bootloaders, Server Setup for Network Boot,Using the U-Boot Bootloader.. | 8 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Device Drivers-Part I:**Introduction, Building and running modules, Char Drivers,Allocating memory. | 7 | 20 |
| VI | **Device Drivers-Part II:** USB Drivers, Device Model, Memory mapping and DMA, Block Drivers, TTY Drivers. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6618 | Functional Verification with SystemVerilog | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the basics of Verification and hardware verification languages.
2. To know the various aspects of SystemVerilog.
3. To understand the features associated with SystemVerilog.
4. To study the concepts of inheritance, constrained randomization and assertions.

## Syllabus

Basics of Verification - Verification Methodologies, Introduction to SystemVerilog- Basics of SystemVerilog language,SystemVerilog operators and functions, Structs, Unions, Arrays, Semaphores and Mailboxes, Class and Extensions- SystemVerilog Classes and inheritance in SystemVerilog, Connecting the Testbench and Design- Interfaces, Program block, Clocking, Constrained Randomization and Coverage, System Verilog assertions.

## Expected Outcome

1. The student who completes this course will be familiarized with the verification methodology followed in VLSI Industry.
2. The student will be able to adapt these to his specific industrial needs, also enable to contribute to the development of more efficient tools for functional verification.

## References

1. Christian B Spear, “SystemVerilog for Verification: A guide to learning the Testbench language features”, Springer publications, 3 rd edition.
2. Sutherland, “ Systemverilog for Design”, Springer publications.
3. SasanIman, "Step-by-Step Functional Verification with SystemVerilog and OVM", Hansen Brown, 2005.
4. Bergeron, Janick, "Writing Testbenches using SystemVerilog", Springer publications, 2006.
5. Vijayaraghavan, Srikanth, Ramanathan, Meyyappan, "A Practical Guide for SystemVerilog Assertions", Springer publications, 2005.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Basics of Verification:** Verification Methodologies, Difference between verification & testing, Test benches, Layered Organization of Test benches, Importance of hardware verification languages and methodologies.**Introduction to SystemVerilog:**SystemVerilog data types, 4-state & 2-state types, typedefs, enum, struct data type. Packages, strings, static and dynamic type casting. | 7 | 15 |
| II | **SystemVerilog operators and functions:** loops in system Verilog, always blocks, tasks and functions case if and if-else statements, time scale.**Structures, Arrays, Semaphores and Mailboxes:**Structs and its assignments, packed and unpacked arrays, associative arrays and methods, queues, semaphores and mailboxes. | 8 | 20 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Class and Extensions :**SystemVerilog class basics, class declaration, class members and methods, class handles, 'super' and 'this' keywords, user defined constructors, class extension/inheritance, new constructors, extending class methods, Virtual class, polymorphism using virtual methods. | 8 | 20 |
| IV | **Connecting the Testbench and Design:**Separating the Testbench and Design, Interface overview.**Program block:** Fundamental testbench construction, program blocks, program block interaction with modules. **Clocking:** Clocking blocks, clocking skews, fork-join processes. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Constrained Randomization and Coverage:** Random variables & built-in-randomization methods, random sequence & examples, Randomization constraints, constraint distribution and set membership, covergroups, coverpoints, coverpoint bins and labels, cross coverage.. | 6 | 15 |
| VI | **SystemVerilog assertions:** Assertion definition, assertion benefits, SystemVerilog assertion types (immediate assertions, concurrent assertions, implications, properties & sequences) Assertion system functions, Assertion severity tasks. | 6 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6622 | High Speed Digital Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the importance of modeling of wires and power distribution for high speed digital design.
2. To understand the concepts of advanced signaling & timing conventions and synchronization.
3. To obtain a clear idea of Ultra fast VLSI Circuits and Systems and the current Technology development.

## Syllabus

Introduction to High Speed Digital Design: modeling and analysis of wires, transmission lines; Power Distribution and Noise: Power supply network-Local power regulation- Logic Loads and on-chip power supply distribution; Noise sources in digital system; Signaling convention and Circuits: Signaling modes, Advanced signaling techniques; terminators; Timing Convention:- Timing fundamentals, Encoding Timing, open loop synchronous Timing, clock Distribution; Synchronization : Synchronization fundamentals, Synchronizer Design; PLL and DLL based lock aligners.

## Expected Outcome

1. The students get familiarized with the system-level electrical design of a digital system.
2. The students get exposed to various aspects of system level design issues which enable them to meet the speed and power requirements of modern integrated circuits.

## References

1. Dally &Paulton, Digital System Engineering, Cambride University Press, 2008.
2. Johnson & Graham, High Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1st Edition.
3. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley, 1st Edition.
4. Jan M.Rabaey et al. Digital Integrated Circuits: A design Perspective, Second Edition, 2003.
5. Douglas A Pucknell& Kamran Eshragian, Basic VLSI Design, PHI, Third Edition.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Introduction to High Speed Digital Design:-**Frequency, time and distance- Capacitance and Inductance Effects- High speed properties of logical gates- Speed and power- modeling and analysis of wires- Geometry and Electrical properties of wires- Electrical model of wires- transmission lines- lossless LC transmission lines- lossy LRC transmission lines – Special transmission lines. | 8 | 20 |
| II | **Power Distribution and Noise:- -** Power supply network-Local power regulation- Logic Loads and on-chip power supply distribution: IR drops- Area bonding- On chip bypass capacitors- Symbiotic bypass capacitors, Power supply isolation ;Noise sources in digital system- Power supply Noise – Cross talk- Intersymbol interference. | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Signaling convention and Circuits:-**Signaling modes for transmission lines- Signaling over lumped transmission media; Advanced signaling techniques: Signaling over RC interconnects- driving lossy LC lines- simultaneous bi-directional Signaling; terminators- transmitter and receiver circuits. | 7 | 15 |
| IV | **Timing Convention:-** Timing fundamentals- Timing properties of clocked storage elements; Encoding Timing: signals and events, encoding aperiodic events & periodic signals, open loop synchronous Timing-Global clock & Edge Triggered timing, level sensitive clocking- pipeline Timing; clock Distribution. | 7 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Open Loop & Closed Loop Timing:** Open loop synchronous Timing - Global clock & Edge Triggered timing, level sensitive clocking, pipeline Timing Closed Loop Timing: Phase comparators. Clock Distribution : Off chip and On Chip Clock distribution | 7 | 15 |
| VI | **Synchronization:** Synchronization fundamentals: Uses of synchronization- Synchronization failure and metastability.**Synchronizer Design:**Mesochronous, Plesiochronous& periodic asynchronous types; PLL and DLL based lock aligners. | 6 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6624 | Nanoelectronics: Devices & Materials | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To get a deep knowledge of nanoelectronics technology and its need in current era.
2. To study the materials used in nanoelectronics, its growth & fabrication & to understand the concepts of different nanostructure devices.

## Syllabus

Review of Microelectronics: Quantum Mechanics: Probability and the Uncertainty Principle- The Schrodinger Wave Equation- Potential Well Problem; E-K Diagrams; MOSFETs: MOSFET Scaling - Short Channel Effect and Narrow Width Effect; High-K gate dielectrics; Nanoelectronics Basics: Potentials of Silicon Technology; Limits of microminiaturization; Basics of Nanoelectronics: Physical fundamentals & Materials -Semiconductor Heterostructures- Organic semiconductors- Carbon Nanomaterials: Nanotubes & Fullerenes; Growth, Fabrication & Measurement Techniques for Nanostructures; Electrons in Traditional Low Dimension Structures; Nanostructure Devices; Ballistic FET; Quantum Electronic Devices & Examples.

## Expected Outcome

1. The student will be able to develop a strong understanding of the concepts of Nanoelectronics technology & quantum mechanics.
2. The student will be familiarized with different nanostructure devices & quantum electronic devices.

## References

1. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.
2. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio,"Introduction to Nanoelectronics: Science, Nanotechnology, Engineering and Applications", Cambridge University press, 2008.
3. Mircea Dragoman and Daniela Dragoman, Nanoelectronics – Principles & devices, Artech House Publishers, 2005.
4. Bharat Bhushan, "Springer Handbook of Nanotechnology", 2nd Edition.
5. Ben.G. Streetman, Solid State Electronic Devices, 5th Edition.
6. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Review of Microelectronics:** Quantum Mechanics: Probability and the Uncertainty Principle- The Schrodinger Wave Equation- Potential Well Problem- Tunneling; Charge Carriers in Semiconductors: E-K Diagrams- Electrons and Holes- Effective Mass- Intrinsic & Extrinsic Material- Electrons and Holes in Quantum Wells; The Fermi Level; MOSFETs: Short Channel MOSFET l-V Characteristics-Control of Threshold Voltage- Substrate Bias Effects- Subthreshold Characteristics- MOSFET Scaling and Hot Electron Effects-DIBL- Short Channel Effect and Narrow Width Effect- GIDL; High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance. | 8 | 20 |
| II | **Nanoelectronics Basics:** On the way to Nanoelectronics; Potentials of Silicon Technology: Base Material-Technologies-Limits of microminiaturization; MEMS; Integrated Optoelectronics; Basics of Nanoelectronics: Physical fundamentals-Basics of Information Theory. | 6 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Materials for Nanoelectronics:** Semiconductors-Crystal Lattices-Electron Energy bands-Semiconductor Heterostructures-Lattice matched &pseudomorphicheterostructures-Organic semiconductors-Carbon Nanomaterials: Nanotubes & Fullerenes. | 6 | 15 |
| IV | **Growth, Fabrication & Measurement Techniques for Nanostructures:** Bulk Crystal &heterostructure Growth-Nanolithography & etching for fabrication of nanostructures &nanodevices-Techniques for characterization of nanostructures-Spontaneous formation & ordering of nanostructures-clusters &nanocrystals-Methods of nanotube growth-chemical & biological methods for nanoscale fabrication-Fabrication of NEMS. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Electron Transport in Semiconductors & Nanostructures:** Time & Length scales of electrons in solids-Statics of electrons in solids & nanostructures-Density of states of electrons & Electron Transport in nanostructures; Electrons in Traditional Low Dimension Structures: | 7 | 15 |

| | | | |
|---|---|---|---|
| | Electrons in Quantum wells, Quantum Wires & Quantum Dots. | | |
| **VI** | **Nanostructure Devices:** Resonant Tunneling Diodes-FET-Single Electron Transfer Devices-Potential Effect Transistors-LED & Lasers-NEMS; Ballistic FET; Quantum Electronics- Quantum Electronic Devices & Examples. | 8 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6692 | Mini Project | **0-0-4** | **2** | **2015** |

## Course Objectives

**To make students**

Design and develop a system or application in the area of their specialization.

## Approach

The student shall present two seminars and submit a report.The first seminar shall highlight the topic, objectives, methodology, design and expected results. The second seminar is the presentation of the work / hardwareimplementation.

## Expected Outcome

Upon successful completion of the miniproject, the student should be able to

1. Identify and solve various problems associated with designing and implementing a system or application.
2. Test the designed system or application.

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC6694 | Advanced Micro Controller Lab | **0-0-2** | **1** | **2015** |

## Course Objectives

1. To understand the architectures of Intel 8051, ARM processor.
2. To familiarize with the design and development process of embedded systems based on these microcontrollers.
3. To familiarize with programming with open source hardware and software tools.

## Syllabus

8- bit Controller – Introduction to IDE – Assembly Language Programming – Addressing modes – Accessing memory using various addressing modes – Instruction set – I/O Port Programs – Arithmetic operations and Programs –Logical operations and Programs – Jump and Call instructions and Programs - Timer and counter - Serial Communication -Connection to RS-232- Serial Communication Programming.

32- bit Controller – ARM – Introduction to embedded OS – Open source tool chain – Open source development board –Basic ARM programming - Linux application – Device Driver

## List of Experiments

Section I: 8- bit Controller - 8051 based microcontroller

1. Assembly level program to toggle the LED connected to Port Pin at 1sec. interval. Use software delay.
   a. Modify the above program for a 25% duty cycle.
2. Assembly level program to display the status of Port Pin in the LED. Connect a switch to a Port Pin to give the input.
3. Interface a seven segment display to the 8051 evaluation board and develop an assembly level program to display 0 – 9 at intervals of 1 second. Use software delay.
4. Assembly level program to configure Timer to create 1 second delay and display 0-9 at the 7-seg display using this delay.
5. Assembly level program to display “P” when switch is pressed& hold, and “L” when switch is released.
6. Assembly level program to display “L” when the switch is pressed and hold for 2 seconds and “S” when key is pressed and hold below 1 second.
7. Assembly level program to display the interval between successive switch presses in seconds on the 7-seg display.
8. Assembly level program to generate one second delay using Timer in interrupt mode. Use

this delay to display 0-9 at the 7-seg LED.
9. Assembly level program to transmit "A" to "Z" to the UART continuously.
10. Assembly level program to transmit "A" if the received data is "X"
11. Assembly level program to store the name of students in the class and their roll nos. Display all the stored information on pressing "Esc" key.

Section II: 32- bit Controller – ARM based microprocessor

1. Bare metal C program to toggle the GPIO on ARM based development board.
2. Linux based C application to toggle the GPIO on ARM based development board.
3. Develop a device driver to toggle the GPIO on ARM based development board.

## Expected Outcome

1. The student will get a strong understanding of general purpose microcontrollers.
2. The student will become familiar about the use of microcontroller in solving real world issues.
3. The student will have hands-on experience in assembly programming and C programming.
4. The student will be familiar with Linux system embedded programming.

## References

1. Ayala Kenneth J, 8051 microcontroller: Architecture, Programming and Application, 3rd edition.
2. Muhammad Ali Mazidi, R.D.Mckinlay, The 8051 Microcontroller and Embedded Systems using Assembly & C, 2nd Edition, Pearson Education.
3. Muhammad Ali Mazidi, R.D.Mckinlay, PIC Microcontroller and Embedded Systems using Assembly & for PIC 18, sixth Edition, Pearson Education.
4. Cortex-M3 Technical Reference Manual, ARM Limited.

# SEMESTER – III

Syllabus and Course Plan

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7611 | Low Power Digital Design | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To get a clear knowledge of emerging low power approaches sources & physics of power dissipation and Power Estimation.
2. To understand the different power analysis methods & methods for Low power design at various design levels.
3. To understand the different clock distribution schemes which are used in Low power design.

## Syllabus

Need for low power VLSI chips, Sources of power dissipation in Digital Integrated circuits, Physics of power dissipation in CMOS devices, Device & Technology Impact on Low Power, Power estimation; Simulation Power analysis: SPICE circuit simulators, Gate level logic simulation, Aarchitecture level analysis, Data correlation analysis in DSP systems. Monte Carlo simulation; Probabilistic power analysis; Low Power Design- Circuit level& Logic level; Low power Architecture & Systems- Power & performance management- low power arithmetic components- low power memory design; Low power Clock Distribution; Algorithm & architectural level methodologies

## Expected Outcome

1. The student will understand the sources of power dissipation and will be able to analyze and estimate power dissipation using the various techniques discussed .
2. On successful completion of the course, the student will be able to apply suitable low power design techniques at different levels of the circuit design.

## References

1. Rabaey, Pedram, "Low power design methodologies" Springer Science & Business Media, 2012.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Need for low power VLSI chips:** Charging & discharging capacitance-short circuit, leakage & static current in CMOS, Basic principles of low power. Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS FET devices. Device & Technology Impact on Low Power-Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. **Power estimation:** Need & Estimation Methods Overview, Signal Modelling& Probability calculation-Estimation of Glitching power-Circuit Reliability & Power Estimation at circuit level-High level power estimation-Information theory based approaches. | 7 | 15 |
| II | **Simulation Power analysis:** SPICE circuit simulation; Gate level logic simulation: capacitive power estimation, static state power, gate level capacitance estimation; architecture level analysis; data correlation analysis in DSP systems; Monte Carlo simulation. | 7 | 15 |
| | **FIRST INTERNAL EXAM** | | |
| III | **Probabilistic power analysis:** Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. | 7 | 15 |
| IV | **Low Power Design- Circuit level:** Transistor & Gate sizing, Network restructuring & organization, Special Latches & flip-flops design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, precomputation logic. | 7 | 15 |
| | **SECOND INTERNAL EXAM** | | |
| V | **Low power Architecture & Systems:**Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. | 7 | 20 |
| VI | **Low power Clock Distribution:**Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock Network. | 7 | 20 |

| | | | |
|---|---|---|---|
| | **Algorithm & Architectural Level Methodologies:**Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. | | |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7613 | VLSI Testing | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the concepts and methodologies in VLSI Testing.
2. To familiarize with the types of faults associated with VLSI fabrication and their diagnosis.
3. To familiarize the concepts of Automatic test pattern generation.

## Syllabus

Basics of testing and fault modeling - Test generation for combinational circuits - Test generation for sequential circuits - Delay fault and IDDQ Testing - Self test and Testable Memory Design - Fault diagnosis.

## Expected Outcome

1. The student who completes this course will be familiar with the various VLSI testing procedures relevant to VLSI Industry from coding level to die level.
2. The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools for VLSI testing at die/package level.

## References

1. P. K. Lala “Digital Circuit Testing and Testability”, Academic Press.
2. Viswani D. Agarval Michael L. Bushnell, "Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit", Kluwer Academic Publications, 1999.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and TestableDesign", Jaico Publishing House, 2002.
4. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice hall International, 2002.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| **I** | **Basics of testing and fault modeling :**Introduction to Testing; Faults in digital circuits; Modeling of faults; Logical Fault Models; Fault detection; Fault Equivalence and location; Fault dominance; Logic and fault Simulation; Types of simulation; Delay models; Gate level Event-driven simulation. | 7 | 15 |

| | | | |
|---|---|---|---|
| **II** | **Test generation for combinational circuits:** Test generation for combinational logic circuits; Testable combinational logic circuit design. | 7 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| **III** | **Test generation for sequential circuits:**Test generation for sequential circuits; design of testable sequential circuits. Boundary Scan - JTAG Fundamentals. | 7 | 15 |
| **IV** | **Delay fault and IDDQ Testing:** Delay test - Path delay test and fault models - Transition faults - delay test methodologies - practical consideration - IDDQ testing - Testing methods - Limitations of IDDQ testing - DFT IDDQ. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| **V** | **Self-test and Testable Memory Design:** Built-In Self-Test; Test pattern generation for BIST ; Circular BIST ; BIST Architectures; Testable Memory Design; Test algorithms; Test generation for Embedded RAMs. | 7 | 20 |
| **VI** | **Fault diagnosis:** Logic Level Diagnosis; Diagnosis by UUT reduction; Fault Diagnosis for Combinational Circuits; Self checking design; System Level Diagnosis. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7615 | Innovative DSP Concepts | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To provide an overview of time frequency analysis and hence the significance of wavelet transform.
2. To familiarize the concepts of parametric modeling for spectral analysis and the estimation /prediction of stationary processes.
3. To familiarize the concepts of band pass sampling on the basis of Hilbert Transforms.
4. To enable the students to use wavelet transforms for applications like data compression.
5. Familiarizes some of the widely used models and algorithms used in aircrafts, spacecrafts, navigation and control of vehicles etc.

## Syllabus

Fourier Analysis of Signals using Discrete Fourier transform - properties of windows, effect of spectral sampling, Time Dependent Fourier Transform and analysis, Parametric Signal Modeling, All Pole Modeling of signals, All Pole Spectrum Analysis, Lattice Filters ,Discrete Hilbert Transforms, Hilbert Transform relationship for complex sequences, band pass sampling ,Random processes, Spectral representation of random signals, Properties of power spectral density, Gaussian Process and White noise process, Principle of Parameter estimation and applications, Criteria of estimation, Baysean estimation : Mean square error and MMSE, Mean Absolute error Kalman filtering, Extended Kalman Filter, Discrete Wavelet Transform, applications of wavelet transform for data compression.

## Expected Outcome

1. The student will gain a better appreciation about linear as well as nonlinear aspects of signal processing.
2. The student will be able to use Wavelet Transforms for applications such as image compression.
3. The student will gain a better vision about the various application domains of DSP.

## References

1. A.V.Oppenheim, R.W .Scafer, Discrete time Signal Processing, Pearson, 3rd edition , 2013.
2. M. Hays: Statistical Digital Signal Processing and Modelling, John Willey and Sons, 1996
3. M.D. Srinath, P.K. Rajasekaran and R. Viswanathan: Statistical Signal Processing with Applications, PHI, 1996.
4. Bopadikar and Rao , Wavelet Transforms, Pearson Education.
5. K.P Soman," Insight into wavelets", PHI.

6. ProakisManolokis Digital Signal Processing - Principles , Algorithms and Applications, , 3rd edition, PHI.
7. D.G. Manolakis, V.K. Ingle and S.M. Kogon: Statistical and Adaptive Signal Processing, McGraw Hill, 2000.
8. G . Stranf , T. Nguyen, Wavelets and Filter Banks, Wellesly- Cambridge.
9. M . Vetterly& J Kovacevic, Wavelets and Subband Coding, Prentice Hall.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Fourier Analysis of Signals using Discrete Fourier transform -** Fourier Analysis of signals using DFT, DFT analysis of Sinusoidal signals-properties of windows, effect of spectral sampling, Time Dependent Fourier Transform, Time Dependent Fourier Analysis of speech signals, Fourier Analysis of stationary random signals, Spectrum Analysis of Random signals. | 7 | 15 |
| II | **Parametric Signal Modeling:** Introduction, All Pole Modeling of signals, Least Square Inverse Model, Deterministic and Random Signal Models, Estimation of Correlation Functions, Model Order, All Pole Spectrum Analysis, Solution of Autocorrelation Normal Equations, Lattice Filters. | 7 | 20 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Discrete Hilbert Transforms:** Introduction, Real and Imaginary Part sufficiency of Fourier Transform, Sufficiency theorems for Finite length Sequences, magnitude and Phase relationships, Hilbert Transform relationship for complex sequences, band pass sampling. | 7 | 15 |
| IV | **Random processes:** Introduction, wide-sense stationary processes, autocorrelation and autocovariance functions, Spectral representation of random signals, Wiener Khinchin theorem Properties of power spectral density, Gaussian Process and White noise process. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Parameter Estimation Theory:**Principle of estimation and applications, Properties of estimates, unbiased and consistent estimators, Minimum Variance Unbiased Estimates (MVUE), Cramer Rao bound, Efficient estimators; Criteria of estimation: the methods of maximum likelihood | 7 | 15 |

| | | | |
|---|---|---|---|
| | and its properties; Baysean estimation : Mean square error and MMSE, Mean Absolute error. | | |
| **VI** | **Kalman Filtering:**State-space model and the optimal state estimation problem, discrete Kalman filter, continuous-time Kalman filter, Extended Kalman Filter.<br>**Discrete Wavelet Transform:** Orthonormal Wavelet Analysis- Filter Bank Implementation, applications of wavelet transform for data compression. | 7 | 20 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7617 | Static Timing Analysis: Constraints & Analysis | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the concepts of Static Timing Analysis in Industry standard digital design flow.
2. To study the concept design constraints in ASIC/FPGA designing.
3. To familiarize the various Timing Analysis Concepts and requirements in practical design flow.

## Syllabus

Introduction-- STA Concepts-- Standard Cell Library-- Interconnect Parasitics-- Delay Calculation-- Crosstalk and Noise-- Configuring the STA Environment-- Timing Verification-- Interface Analysis-- Robust Verification.

## Expected Outcome

1. The student who completes this course will be familiarized with the concepts of Static Timing Analysis relevant to nanometer designs.
2. The student will be able to adapt these to his specific industrial needs, also contribute to the development of more efficient tools for STA.

## References

1. J.Bhasker, RakeshChadha, "Static Timing Analysis for Nanometer Designs, A practical approach", Springer publications.
2. Gangadharan, Sridhar, Churiwala, Sanjay "Constraining Designs for Synthesis and Timing Analysis": A Practical Guide to Synopsys Design Constraints (SDC), Springer publications.
3. Churiwala, Sanjay, Garg, Sapan "Principles of VLSI RTL Design" A Practical Guide, Springer publications.
4. Maheshwari, Naresh, Sapatnekar, S. "Timing Analysis and Optimization of Sequential Circuits" Springer publications.
5. HimanshuBhatnagar "Advanced ASIC Chip Synthesis" Using Synopsys Design Compiler Physical Compiler and PrimeTime, Springer publications.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Introduction:**Basics; Crosstalk and Noise, Design Flow ; CMOS, FPGA & Asynchronous Designs; STA at Different Phases; Limitations; Power& Reliability Considerations .**STA Concepts:**CMOS Logic; Modeling of CMOS Cells; Switching Waveform; Propagation Delay; Slew of a Waveform ;Skew between Signals; Timing Arcs and Unateness; Min and Max Timing Paths; Clock Domains; Operating Conditions. | 7 | 15 |
| II | **Standard Cell Library:**Pin Capacitance; Timing Modeling; Timing Models - Combinational Cells; Timing Models - Sequential Cells; State-Dependent Models; Interface Timing Model for a Black Box; Advanced Timing Modeling; Power Dissipation Modeling; Other Attributes in Cell Library; Characterization and Operating Conditions. | 7 | 20 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Interconnect Parasitics:**RLC for Interconnect;Wireload Models; Representation of Extracted Parasitics; Representing Coupling Capacitances; Hierarchical Methodology; Reducing Parasitics for Critical Nets**Delay Calculation:**Overview; Cell Delay using Effective Capacitance; Interconnect Delay; Slew Merging; Different Slew Thresholds; Different Voltage Domains; Path Delay Calculation; Slack Calculation. | 7 | 20 |
| IV | **Crosstalk and Noise:**Overview; Crosstalk Glitch Analysis; Crosstalk Delay Analysis; Timing Verification Using Crosstalk Delay; Computational Complexity; Noise Avoidance Techniques. **Configuring the STA Environment:**Specifying Clocks; Generated Clocks; Constraining Input Paths; Constraining Output Paths; Timing Path Groups; Modeling of External Attributes; Design Rule Checks; Virtual Clocks; Refining the Timing Analysis; Point-to-Point Specification; Path Segmentation. | 7 | 15 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Timing Verification:**Setup Timing Check; Hold Timing Check; Multicycle Paths; False Paths; Half-Cycle Paths; Removal Timing Check; Recovery Timing Check; Timing across Clock Domains; Examples; Multiple Clocks**Interface Analysis:** IO Interfaces; SRAM Interface. | 7 | 15 |
| VI | **Robust Verification:** On-Chip Variations; Time Borrowing; Data to Data Checks; Non-Sequential Checks; Clock Gating Checks; Power Management; Backannotation; Sign-off Methodology. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7619 | Nanoscale Transistors | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To understand the physics and effects of nanoscalemultigate transistors in detail.
2. To understand the concepts of Carbon Nanotube FETs & SETs.
3. To familiarize with Graphene Technology & GFETs.

## Syllabus

Review of MOSFETS & Introduction to Nanoscale effects: MOSFET physics & I-V Characteristics-MOSFET Scaling &penalities. Nanoscale Effects: Gate Oxide leakage currents: Gate Oxide Tunneling & Impact-Models for QMDT in Gate OxidesTunneling in Multiple Gate MOSFETs; Inversion Layer Quantization- Dielectrics for Nanoelectronics; The SOI MOSFET; Multigate MOSFET Technology; Physics of Multigate MOS system, Transistor Models- Mobility in Multigate MOSFETs-Double Gate MOSFETS &FinFETS; Radiation effects in Single &Multigate SOI MOSFETs- Multigate MOSFET circuit Design: Digital circuit design-Analog circuit design; Nanowire FETs: Silicon Nanowire MOSFETs-Carbon Nanotubes- Carbon nanotube FETs & MOSFETs; Transistors at molecular scale: Model for Ballistic Nanotransistors-MOSFETs with 0D,1D & 2D channels-Molecular Transistors-Single Electron Transistors.

## Expected Outcome

1. The student will be able to develop a strong understanding of the concepts of different types of nanoscale transistors & the factors affecting it.
2. The student will be familiarized with the GFETs & the challenges facing in current Graphene technology.

## References

1. J P Colinge, “FINFETs and other multi-gate transistors”, Springer – Series on integrated circuits and systems, 2008.
2. AmitChaudhry, “Fundamentals of Nanoscaled Field Effect Transistors”, Springer, 2013.
3. Mark Lundstrom Jing Guo, “Nanoscale Transistors: Device Physics, Modeling and Simulation”, Springer, 2006.
4. Raghu Murali, “GrapheneNanoelectronics: From Materials to Circuits”, Springer, 2012.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Review of MOSFETS & Introduction to Nanoscale effects:** MOSFET physics & I-V Characteristics-MOSFET Scaling-Penalties of scaling. **Nanoscale Effects:** Gate Oxide leakage currents: Gate Oxide Tunneling & Impact-Models for QMDT in Gate Oxides-Impact of parameters on QMDT current density-Tunneling in Multiple Gate MOSFETs; Inversion Layer Quantization: Inversion Layer Quantization in substrate-Modeling approaches-Existing models-Effect on Threshold voltage & Drain current; Dielectrics for Nanoelectronics. | 6 | 15 |
| II | **The SOI MOSFET:** Brief History of Multiple-Gate MOSFETs, Multigate MOSFET physics.<br>**Multigate MOSFET Technology:** Active area-Fins, - Gate stack-Source/Drain resistance & capacitance-Mobility & Strain engineering-Contacts to the Fins. | 7 | 15 |
| | **FIRST INTERNAL EXAM** | | |
| III | **Physics of Multigate MOS system, Transistor Models:** Device electrostatics-Double Gate MOS system-2D confinement; A brief study on Multigate Transistor models-BSIM-CMG & BSIM-IMG; Mobility in MultigateMOSFETs:Double Gate MOSFETS &FinFETS: Photon limited mobility-interface roughness & coulomb scattering-Temperature dependence on mobility-high-k dielectrics; Silicon Multiple-gate Nanowires. | 7 | 15 |
| IV | **Radiation effects in Single &Multigate SOI MOSFETs:** Total Ionizing Dose effects-Single Event effects.**Multigate MOSFET circuit Design:** Digital circuit design-Analog circuit design. | 8 | 20 |
| | **SECOND INTERNAL EXAM** | | |
| V | **Nanowire FETs:** Silicon Nanowire MOSFETs-Carbon Nanotubes-Band structure of carbon nanotubes-Carbon nanotube FETs & MOSFETs-Schotkey barrier Carbon Nanotube FETs.**Transistors at molecular scale:** Electron conduction in molecules-Model for Ballistic Nanotransistors-MOSFETs with 0D,1D & 2D channels-Molecular Transistors-Single | 8 | 20 |

| | | | |
|---|---|---|---|
| | Electron Transistors. | | |
| **VI** | **Graphene Technology & GFETs:** Evolution of Graphene Technology-Electronic transport in Graphene-Technical Challenges in GFETs-graphene Transistors-Formation of Epitaxial Graphene-Graphene Growth by CVD methods-Graphene FET Models. | 6 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7621 | VLLSI Design Automation | **3-0-0** | **3** | **2015** |

## Course Objectives

1. To study different shortest path algorithms and N-P Complete problem in detail.
2. To understand the concepts of placement, floor planning & routing, its problem formulation and algorithms concerned.

## Syllabus

Graph Algorithms: Data structures for Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm, Shortest path Algorithm , Min cut and Max cut Algorithms; N-P complete Problem; Logic synthesis & verification; Compaction-1D and 2D; VLSI automation Algorithms- Partitioning: problem formulation, classification of partitioning algorithms; Placement, floor planning & pin assignment: problem formulation, placement algorithms; Global Routing: problem formulation & routing algorithms; Detailed routing: problem formulation & routing algorithms.

## Expected Outcome

1. The student will get a deep knowledge about the different shortest path algorithms and the concepts of problem formulation of floor planning, placement and routing.
2. The student who successfully completes this course will be able to apply the apt algorithm in the areas of floor planning, placement & routing when go for a design.

## References

1. NaveedShervani, Algorithms for VLSI physical design Automation, Kluwer Academic Publisher, Third edition.
2. Sabih H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, Second Edition, 2008.
3. ChristophnMeinel& Thorsten Theobold, Algorithm and Data Structures for VLSI Design, KAP, 2002.
4. Rolf Drechsheler, Evolutionary Algorithm for VLSI, Second edition.
5. Trimburger, Introduction to CAD for VLSI, Kluwer Academic publisher, 2002.
6. T .H. Cormen, C. E. Leiserson, R. L. Rivest , Introduction to Algorithms, PHI.

## COURSE PLAN

| Module | Contents | Hours Allotted | % of Marks in End-Semester Examination |
|---|---|---|---|
| I | **Graph Algorithms:**Data structures for Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Spanning Tree Algorithm - Kruskal's and Prim's, Shortest path Algorithm - Dijkstra's and Bellman Fort Algorithm for single pair Shortest paths, Floyd-Warshall algorithm for All pair Shortest path, Matrix multiplication modeling of All pairs shortest path problem, Min cut and Max cut Algorithms | 7 | 15 |
| II | **N-P complete Problem:**Polynomial time non-deterministic algorithm, N-P completeness and reducibility, Proof and problems. **Logic synthesis & verification:** Introduction to combinationallogic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis. Allocation, assignment and scheduling. | 6 | 15 |
| **FIRST INTERNAL EXAM** | | | |
| III | **Compaction:**problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction. **VLSI automation Algorithms:** Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. | 8 | 20 |
| IV | **Placement, floor planning & pin assignment:**problem formulation, placement algorithms, floor planning concepts, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment. | 8 | 20 |
| **SECOND INTERNAL EXAM** | | | |
| V | **Global Routing:**Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches. | 6 | 15 |
| VI | **Detailed routing:**problem formulation, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization. | 7 | 15 |
| **END SEMESTER EXAM** | | | |

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7691 | Seminar II | **0-0-2** | **2** | **2015** |

## Course Objectives

To make students

1. Identify the current topics in the specific stream.
2. Collect the recent publications related to the identified topics.
3. Do a detailed study of a selected topic based on current journals, published papers and books.
4. Present a seminar on the selected topic on which a detailed study has been done.
5. Improve the writing and presentation skills.

## Approach

Students shall make a presentation for 20-25 minutes based on the detailed study of the topic and submit a report based on the study.

## Expected Outcome

Upon successful completion of the seminar, the student should be able to

1. Get good exposure in the current topics in the specific stream.
2. Improve the writing and presentation skills.
3. Explore domains of interest so as to pursue the course project.

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7693 | Project (Phase I) | **0-0-12** | **6** | **2015** |

## Course Objectives

To make students

1. **Do an original and independent study on the area of specialization.**
2. **Explore in depth a subject of his/her own choice.**
3. **Start the preliminary background studies towards the project by conducting literature survey in the relevant field.**
4. Broadly identify the area of the project work, familiarize with the tools required for the design and analysis of the project.
5. Plan the experimental platform, if any, required for project work.

## Approach

The student has to present two seminars and submit an interim Project report. The first seminar would highlight the topic, objectives, methodology and expected results. The first seminar shall be conducted in the first half of this semester. The second seminar is the presentation of the interim project report of the work completed and scope of the work which has to be accomplished in the fourth semester.

## Expected Outcome

Upon successful completion of the project phase 1, the student should be able to

1. Identify the topic, objectives and methodology to carry out the project.
2. **Finalize the project plan for their course project.**

# SEMESTER - IV

Syllabus and Course Plan

| Course No. | Course Name | L-T-P | Credits | Year of Introduction |
|---|---|---|---|---|
| 01EC7694 | Project (Phase II) | **0-0-23** | **12** | **2015** |

## Course Objectives

To continue and complete the project work identified in project phase 1.

## Approach

There shall be two seminars (a mid term evaluation on the progress of the work and pre submission seminar to assess the quality and quantum of the work). At least one technical paper has to be prepared for possible publication in journals / conferences based on their project work.

## Expected Outcome

Upon successful completion of the project phase II, the student should be able to

1. Get a good exposure to a domain of interest.
2. Get a good domain and experience to pursue future research activities.